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QUESTION BANK (DESCRIPTIVE)

Subject with Code : STLD(19EC0401) **Course & Branch**: B.Tech - ECE

Year & Sem: I-B.Tech & II-Sem

UNIT –I

BINARY SYSTEMS, BOOLEAN ALGEBRA & LOGIC GATES

1. Convert the given decimal number 234 to binary, quaternary, octal, hexadecimal and BCD equivalent. **(10M)L1, CO.1**
2. Perform the following
   a) Subtraction by using 10's complement for the given 3456 - 245. **(5M)L3, CO.1**
   b) Subtraction by using 2's complement for the given 111001-1010. **(5M)L3, CO.1**
3. a) Convert the following to Decimal and then to Octal. (i) $(42341)_6$ (ii) $(10010011)_2$. **(5M)L1, CO.1**
   b) Convert the following to Decimal and then to Hexadecimal. (i) $(1234)_8$ (ii) 11001111_2 **(5M)L1, CO.1**
4. Simplify the following Boolean expression:
   (a) F = (A+B)(A'+C)(B+C). **(5M)L3, CO.1**
   (b) F = A+B+C'+D(E+F) **(5M)L3, CO.1**
5. a) Obtain the truth table of the following Boolean function and express the function as sum of minterms and product of maxterms F = (A+B) (B+C) **(5M)L3, CO.1**
   b) Simplify the following Boolean functions to minimum number of literals **(5M)L3, CO.1**
   (i) xyz + x'y + xyz'. (ii) xz + x'yz.
6. Convert the following to Decimal and then to Octal **(10M)L1, CO.1**
   (a) 1234_{16} (b) $12EF_{16}$ (c) 10110011_2 (d) 10001111_2 (e) 352_{10}
   (f) 999_{10}
7. a) Simplify the following Boolean expressions to minimum no. of literals. **(5M)L3, CO.1**
   i. ABC+A'B+ABC' ii. (BC'+A'D)(AB'+CD')
   iii. x'yz+xz iv. xy+x(wz+wz')
   b) Obtain the Dual of the following Boolean expressions. **(5M)L3, CO.1**
   i. AB+A(B+C)+B'(B+D) ii. A+B+A'B'C
   iii. A'B+A'BC'+A'BCD+A'BC'D'E iv. ABEF+ABE'F'+A'B'EF
8. (a) State Duality theorem. List Boolean laws and their Duals. **(5M)L1, CO.1**
   (b) Simplify the following Boolean functions to minimum number of literals: **(5M)L3, CO.1**
   i. F = ABC + ABC' + A'B ii. F = (A+B)' (A'+B')
9. a) Convert the following to binary and then to gray code. **(5M)L1, CO.1**
   (i) $(1111)_{16}$ (ii) $(BC54)_{16}$ (iii) $(237)_8$ (iv) $(164)_{10}$ (v) $(323)_8$
   b) Perform the following using BCD arithmetic **(5M)L3, CO.1**
   (i) $(79)_{10} + (177)_{10}$ (ii) $(481)_{10} + (178)_{10}$
10. Convert the following to gray code and then to binary. **(10M)L1, CO.1**
    (a) $(1111)_{16}$ (b) $(BC54)_{16}$ (c) $(237)_8$ (d) $(164)_{10}$ (e) $(323)_8$

UNIT –II

GATE -LEVEL MINIMIZATION

1. a) Minimize the following Boolean function using K-Map **(5M)L2, CO.1**
   F(A, B, C, D)= Σm(0, 2, 4, 6, 8, 10, 12, 14).
   b) Realize it using NAND Gates. **(5M)L2, CO.1**
2. Minimize the given Boolean function F(A,B,C,D) = Σ m(0,1,2,3,6,7,13,15) using tabulation method and implement using basic gates **(10M)L2, CO.1**
3. a) Simplify the following Boolean expressions using K-map **(5M)L3, CO.1**
   F(W,X,Y,Z)= XZ+W'XY'+WXY+W'YZ+WY'Z
   b) Implement the same using NAND gates. **(5M)L3, CO.1**
4. Simplifying the following expression using tabulation technique. **(10M)L3, CO.1**
   F=Σm(0,1,2,8,9,15,17,21,24,25,27,31)
5. a) Simplify the following expression using the K-map for the 3-variable. **(5M)L3, CO.1**
   Y = AB'C+A'BC+A'B'C+A'B'C'+AB'C'
   b) Simplify the Boolean function F(A,B,C,D)=∑(1,3,7,11,15)+d(0,2,5) **(5M)L3, CO.1**
6. a) Implement the following Boolean function using NOR gates. **(5M)L3, CO.1**
   Y=(AB'+A'B)(C+D').
   b) Simplify the following Boolean function for minimal POS form using K-map
   F(X,Y,Z) = X'YZ + XY'Z' + XYZ + XYZ' **(5M)L3, CO.1**
7. Simplify the Boolean function by using tabulation method **(10M)L3, CO.1**
   F(a,b,c,d)=Σm(0,1,2,5,6,7,8,9,10,14)
8. Simplify the following Boolean function in POS form using K-map **(10M)L3, CO.1**
   F(A,B,C,D) = Σ(1,2,4,5,9,12,13,14)
9. Simplify the following Boolean function using Tabulation method **(10M)L3, CO.1**
   Y(A,B,C,D) = Σ(1,3,5,8,9,11,15)
10. a) Write the advantages of Tabulation method over K-Map method. **(2M)L5, CO.1**
    b) Write the given Boolean expression f = A+B in Sum of minterms. **(2M)L5, CO.1**
    c) SOP of F(x, y, z)=Σ(2, 3, 6, 7). **(2M)L3, CO.1**
    d) Implement OR gate using only two input NAND gates **(2M)L3, CO.1**
    e) Implement the following Boolean equation using only NAND gates Y=AB+CDE+F. **(2M)L3, CO.1**

UNIT –III

COMBINATIONAL LOGIC

1. a) Design & implement a 4-bit Binary-To-Gray code converter. **(5M)L1, L3 CO.2**
   b) Design a 4 bit binary-to-BCD code converter **(5M)L1, L3 CO.2**
2. a) Design & implement BCD to Excess-3 code converter. **(5M)L1, L3 CO.2**
   b) Design 32:1 Mux using two 16:1 Muxs and one 2:1 Mux. **(5M)L1, L3 CO.2**
3. a) Design & implement Full Adder with truth table. **(5M)L1, L3 CO.2**
   b) Design & implement Full Subtractor with truth table. **(5M)L1, L3 CO.2**
4. Explain Carry Look Ahead Adder circuit with the help of logic diagram. **(10M)L2, CO.2**
5. Construct a BCD Adder-circuit. **(10M)L2, CO.2**
6. Implement 4-bit Magnitude Comparator and write down its design procedure. **(10M)L3, CO.2**
7. a) Design & implement Full Adder using Decoder. **(4M)L1,L3 CO.2**
   b) Implement a 2-bit Magnitude comparator and write down its design procedure. **(6M)L1,L3 CO.2**
8. What is encoder? Design octal to binary encoder. **(10M)L1, CO.2**
9. a) Implement the following Boolean function using 8:1 multiplexer. **(5M)L3, CO.2**

   F(A,B,C,D) = A'BD'+ACD+B'CD+A'C'D.

   b) What is multiplexer? Construct 4*1 multiplexer with logic gates and truth table **(5M)L3, CO.2**
10. a) Draw the basic structure of combinational logic circuit **(2M)L3, CO.2**
    b) Design the full adder using half adders **(2M)L1, CO.2**
    c) Implement 2-bit by 2-bit multiplier with half adders **(2M)L3, CO.2**
    d) Realize a 2-bit comparator using gates **(2M)L3, CO.2**
    e) What is priority encoder? Mention its operation **(2M)L1, CO.2**

UNIT –IV

SYNCHRONOUS SEQUENTIAL LOGIC

1. a) Design D Flip Flop by using SR Flip Flop and draw the timing diagram. **(5M)L1, CO.2**
   b) Write the differences between combinational and sequential circuits. **(5M)L5, CO.2**
2. a) Draw the logic symbol, characteristics table and derive characteristics equation of JK flip flop. **(5M)L3, CO.2**
   b) Design T Flip Flop by using JK Flip Flop and draw the timing diagram. **(5M)L1, CO.2**
3. a) Draw the circuit of JK flip flop using NAND gates and explain its operation. **(5M)L3, CO.2**
   b) Design a 2-input 2-output detector which produces an output 1 every time the sequence 0101 is detected. Implement the sequence detector using JK flip-flops. **(5M)L1, CO.2**
4. a) Convert S-R flip flop into JK-flip flop. Draw and explain the logic diagram. **(5M)L1, CO.2**
   b) A clocked sequential circuit with single input x and single output z produces an output z=1 whenever the input x compares the sequence 1011 and overlapping is allowed. Obtain the state diagram, state table and design the circuit with D flip-flops. **(5M)L3, CO.2**
5. A sequential circuit with two D-flip flops A and B, two inputs ‘x’ and ‘y’ and one output ‘z’ is specified by the following next state and output equation. **(10M)L3, CO.2**

   $A(t+1) = x'y+xA$, $B(t+1) = x'B+xA$ and $Z = B$

   i) Draw the logic diagram of the circuit.
   ii) List the state table and draw the corresponding state diagram
6. Design and implement 3-bit ripple counter using J-K flip flop. Draw the state diagram, logic diagram and timing diagram for the same. **(10M)L1,L3, CO.2**
7. With a neat sketch explain MOD 6 Johnson counter using D FF. **IES 2015** **(10M)L3, CO.2**
8. Implement 6-bit ring counter using suitable shift register. Briefly describe its operation. **(10M)L3, CO.2**
9. Design a binary counter having repeated binary sequence using JK flip flops :0,1,2,4,5,6. **(10M)L1, CO.2**
10. a) Differentiate a Latch with a Flip flop. **(2M)L5, CO.2**
    b) List asynchronous inputs of a sequential device **(2M)L1, CO.2**
    c) Draw the block diagram of sequential circuit using combinational circuit and memory unit. **(2M)L3, CO.2**
    d) Draw the logic circuit of flip-flop and truth table using NOR gates. **(2M)L3, CO.2**
    e) Give the comparison between combinational circuits and sequential circuits. **(2M)L1, CO.2**

UNIT –V
FINITE STATE MACHINES & PROGRAMMABLE MEMORIES

1. Implement the following Boolean function using PLA **(10M)L3, CO.3**
   (i)F(w,x,y,z) = Σm(0,1,3,5,9,13) (ii)F(w,x,y,z)) = Σm(0,2,4,5,7,9,11,15)
2. Implement the following Boolean function usingPAL. **(10M)L3, CO.3**
   (i)A(w,x,y,z) = Σm(0,2,6,7,8,9,12,13) (ii)B(w,x,y,z)) = Σm(0,2,6,7,8,9,12,13,14)
   (iii)C(w,x,y,z) = Σm(1,3,4,6,10,12,13) (iv)D(w,x,y,z)) = Σm(1,3,4,6,9,12,14)
3. Implement the following Boolean function usingPLA **(10M)L3, CO.3**
   (i)F1= Σm(0,1,2,3,8,10,12,14) (ii)F2 = Σm(0,1,2,3,4,6,8,10,12,14).
4. Implement PLA circuit for the following functions F1(A,B,C)= Σm(3,5,6,7), F2(A,B,C)= Σm(0,2,4,7). **(5M)L3, CO.3**
5. Discuss Mealy & Moore Machine models of sequential machines. **(10M)L1, CO.2**
6. Explain the minimization procedure for determining the set of equivalent state of a specified machine M. **(10M)L2, CO.2**
7. Explain the following related to sequential circuits with suitable examples.
   a)State diagram **(2M)L1, CO.1**
   b) State table **(2M)L1, CO.1**
   c) State assignment **(6M)L1, CO.1**
8. a) Differentiate among ROM, PROM ,DROM ,EPROM, EEPROM, RAM. **(5M)L3, CO.3**
   b) Explain about memory decoding. **(5M)L3, CO.3**
9. Given the 8-bit data word 01011011,generate the 12-bit composite word for the hamming code that corrects and detects single errors. **(10M)L3, CO.3**
10. Give the logic implementation of a 32x4 bit ROM using a decoder of a suitable figure. **(10M)L3, CO.3**